

## UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

DATE MAILED: 08/11/2005

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
09/988,896	11/19/2001	Andy P. Annadurai	021067-000200US	9182
20350	7590 08/11/2005	5	EXAMINER	
	D AND TOWNSEN RCADERO CENTER	JONES, PRENELL P		
	HTH FLOOR		ART UNIT	PAPER NUMBER
SAN FRANCISCO, CA 94111-3834			2667	

Please find below and/or attached an Office communication concerning this application or proceeding.

•	Application No.	Applicant(s)					
	09/988,896	ANNADURAI ET AL.					
Office Action Summary	Examiner	Art Unit					
	Prenell P. Jones	2667					
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address					
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	86(a). In no event, however, may a reply be time within the statutory minimum of thirty (30) days rill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	nely filed s will be considered timety. the mailing date of this communication. D (35 U.S.C. § 133).					
Status							
1) Responsive to communication(s) filed on 11/19	<u>//01</u> .						
<u>,                                    </u>	This action is <b>FINAL</b> . 2b)⊠ This action is non-final.						
·	· · · · · · · · · · · · · · · · · ·						
closed in accordance with the practice under E	x parte Quayle, 1935 C.D. 11, 45	53 O.G. 213.					
Disposition of Claims							
4)⊠ Claim(s) <u>1-19</u> is/are pending in the application.							
4a) Of the above claim(s) is/are withdrawn from consideration.							
5) Claim(s) <u>7-11 and 14-19</u> is/are allowed.							
6)⊠ Claim(s) <u>1-6</u> is/are rejected.	S)⊠ Claim(s) <u>1-6</u> is/are rejected.						
7) Claim(s) 13 is/are objected to.							
8) Claim(s) are subject to restriction and/or	election requirement.						
Application Papers							
9) The specification is objected to by the Examine	r.						
10) The drawing(s) filed on is/are: a) acce		Examiner.					
Applicant may not request that any objection to the	drawing(s) be held in abeyance. See	e 37 CFR 1.85(a).					
Replacement drawing sheet(s) including the correcti	on is required if the drawing(s) is obj	ected to. See 37 CFR 1.121(d).					
11)☐ The oath or declaration is objected to by the Ex	aminer. Note the attached Office	Action or form PTO-152.					
Priority under 35 U.S.C. § 119							
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of:	priority under 35 U.S.C. § 119(a)	-(d) or (f).					
1. Certified copies of the priority documents	s have been received.						
<ol><li>Certified copies of the priority documents</li></ol>	have been received in Application	on No					
<ol><li>Copies of the certified copies of the prior</li></ol>	ity documents have been receive	ed in this National Stage					
application from the International Bureau	• • • • • • • • • • • • • • • • • • • •						
* See the attached detailed Office action for a list of	of the certified copies not receive	d.					
Attachment(s)							
1) Notice of References Cited (PTO-892)	4) Interview Summary						
<ul> <li>2) Notice of Draftsperson's Patent Drawing Review (PTO-948)</li> <li>3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)</li> <li>Paper No(s)/Mail Date</li></ul>	Paper No(s)/Mail Da 5)  Notice of Informal Pa 6) Other:	ite atent Application (PTO-152)					

Application/Control Number: 09/988,896

Art Unit: 2667

## Claim Rejections - 35 USC § 112

- 1. The following is a quotation of the second paragraph of 35 U.S.C. 112:
  - The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.
- 2. Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
- 3. Regarding claim 1, Applicant is claiming in lines 8, 12-13 and 16 "the no skew input", "the late skew input" and "the early skew input" respectively, whereby the stated definition/description in parenthesis () is not recognized as being a positive limitation of the claimed invention. Claims 2-6 depend on claim 1 therefore claims 2-6 are rejected for the same reason that claim 1 is rejected.

## Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 5. Claim 12 is rejected under 35 U.S.C. 102(b) as being anticipated by Forsmo.

Art Unit: 2667

Regarding claim 12, Forsmo discloses a data arriving on a data bus that is associated with a de-skewing circuitry that consist of multiplexing logic having a single output port, a data select port, first, second and third data input ports (Fig. 5A, deskewing circuit that has plurality of registers/first, second and third registers daisy chained communicating via a data bus (106), col. 7, line 28 thru col. 8, line 17), first register, having a data input port coupling to data-bus and a output port for coupling to a first data input port of the multiplexing (mux) logic (Fig. 5A, first register (206a) is indirectly coupled to bus (106) and the first data input port (p0) of the mux via 212a), second register, having a data input port coupling to the data output port of the first register, having a data output port for coupling to the second data input port of the multiplexing logic (Fig. 5A, second register (206b) input coupled to output port of 206a and indirectly coupled to the second input port of mux (p1) via 212b), third register, having a data input port coupling to the data output port of the second register, and a data output port for coupling to the third data input port of the multiplexing logic (Fig. 5A, third register (206c) input is coupled to output port of second register (206b) and indirectly coupled to third input port (p2) of mux via 212c) the multiplex logic receiving first, second, third data input signals from the data output ports of first, second and third registers, and selectively forwarding any one of the first, second and third data input signals to its single output port (Fig. 5, the outputs of first, second, third registers (206a, 206b, 206c) are indirectly coupled to the data selector of mux via controller 230.

Application/Control Number: 09/988,896 Page 4

Art Unit: 2667

## Allowable Subject Matter

1. Claims 7-11 and 14-19 are allowed over prior art.

- 2. Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 3. The following is a statement of reasons for the indication of allowable subject matter: Although the combined prior art of Collins who teaches an architecture that includes multiple latches coupled to a mux and encryption means that performs communicating data between transmitter and receiver, de-skewing and skewing communication channels which are coupled to delay stacks, Shaffer et al who teaches a de-skewing method as associated in a SONET environment wherein the architecture includes a framer, Pickering et al who teaches de-skewing circuits that utilize phase detectors, and the skewing and delays are monitored, Hendrickson et al who teaches a de-skewing method and system associated with parallel data lines wherein the architecture includes multiple channels, controller connected to selectors wherein the processor could be a framer associated in a SONET environment and Clements et al. who teaches consist of data arriving on a data bus that is associated with a de-skewing circuitry that consist plurality of latches connected via a data bus whereby delay and clock data is monitored, compared, adjusted, selected and transmitted, they fail to teach or suggest multiplexer selecting a first data input signal if there exist a late skew at the

Application/Control Number: 09/988,896

Art. Unit: 2667

data bus, or selecting the second data input signal if there is no data skew, or selecting a third data input if an early skew exist.

Page 5

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prenell P. Jones whose telephone number is 571-272-3180. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Prenell P. Jones

August 5, 2005 (

CHI PHAN

SUPERVISORY PATENT EXAMINE

TECHNOLOGY CENTER PROF